AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

Claim **1** (currently amended) A testing method for semiconductor integrated circuits ~~wherein~~, ~~in the~~ said testing method testing by a semiconductor testing apparatus having a comparison judgment circuit judging a semiconductor integrated circuit integrated with a plurality of DA converters and a base voltage generation circuit determining ~~the~~ gradation output voltage characteristics, by comparison of ~~the~~ gradation output voltages of the semiconductor integrated circuit and reference voltages, ~~wherein~~ comprising:

deciding ~~the~~ gradation level intervals to be the test objects ~~are decided~~ by the setting of different voltages to be applied at the base power supply input terminals of said base voltage generation circuit; ~~and~~

supplying said gradation output voltages ~~are supplied~~ at and between said voltages applied to said base power supply input terminals from said semiconductor testing apparatus; and

based on a ~~by assigning~~ correspondence between ~~the~~ input gradation data signals of the gradation levels ~~of that~~ for a gradation level interval, and the gradation output voltages, testing the gradation output voltage ~~testing~~ through said semiconductor testing apparatus ~~is made to be~~ by making a digital judgment.

Claim **2** (currently amended) A testing method for semiconductor integrated circuits according to claim **1**, wherein,

according to the gradation output voltages provided at and between the voltages applied to said base power supply input terminals from said semiconductor testing apparatus, said base

voltage generation circuit increases or decreases the neighboring gradation output potential differences of every analog voltage output of said semiconductor integrated circuit.

Claim 3 (previously presented) A testing method for semiconductor integrated circuits according to claim **1**, wherein,

by assigning correspondence between the voltage settings provided from said semiconductor testing apparatus and the input data, said DA converters and the base voltage generation circuit selectively test the output levels of the analog voltage outputs.

Claim 4 (currently amended) A testing method for semiconductor integrated circuits according to claim **1**, wherein,

~~proving of the~~ reliability of the test accuracy ~~is made possible~~ is acomplished by treating the mutual relationship between the computation of the input data corresponding to every output voltage level and of ~~the~~ expectation values of the output voltages in ~~the~~ a semiconductor integrated circuit specification and ~~the~~ setting of the output voltage expectation value levels, and ~~the~~ voltage judgment value levels of said comparison judgment circuit carrying out the judgment of the output voltages, and

~~the~~ change of the setting of the test numbers with time, altogether as address or parameter management.

Claim 5 (currently amended) A testing device for semiconductor integrated circuits, ~~wherein~~, comprising:

in a judging testing apparatus, through a comparison judgment circuit, a semiconductor integrated circuit integrated with a plurality of DA converters and

a base voltage generation circuit determining the gradation output voltage characteristics, by comparison of said gradation output voltages and reference voltages, wherein

different voltages are output to the base power supply input terminal for the end of one side of the gradation level interval being the test object of said semiconductor integrated circuit, and the base power supply input terminal of the other end of said interval.

Claim **6** (previously presented) A testing device for semiconductor integrated circuits according to claim **5**, wherein,

said voltages are output to more than two base power supply input terminals including the base power supply input terminal at the end of at least one side of the gradation level interval being the test object of the semiconductor integrated circuits.

Claim **7** (previously presented) A testing device for semiconductor integrated circuits according to claim **5**, wherein,

base power supply input terminals not connected with the semiconductor testing apparatus are disposed in the gradation level interval being the test object of the semiconductor integrated circuit.

Claim **8** (previously presented) A testing device for semiconductor integrated circuits according to claim **5**, wherein,

more than two gradation level intervals being the test objects of the semiconductor integrated circuits are disposed.

Claim **9** (canceled).

Claim **10** (canceled).

Claim **11** (new) A testing system for a display semiconductor integrated circuit, comprising:

a tester power supply supplying a plurality of different input voltages;

said semiconductor integrated circuit comprising:

a plurality of base power supply input terminals, a pair of said base power supply input terminals receiving said respective different input voltages,

a base voltage generation circuit, and

a plurality of DA converters,

said base voltage generation circuit and plurality of DA converters generating gradation output voltage characteristics in between the pair of base power supply input terminals as a test object; and

a comparison judgment circuit comparing said gradation output voltages and reference voltages, wherein each gradation output voltage has a corresponding judgment level.

Claim **12** (new) A testing system for a display semiconductor integrated circuit outputting a plurality of gradation output voltages over a graduation level interval, comprising:

a tester power supply supplying a plurality of different input voltages to said semiconductor integrated circuit; and

a comparison judgment circuit comparing said gradation output voltages and reference voltages, wherein each gradation output voltage has a corresponding judgment level;

said tester power supply supplying a first input voltage corresponding to one end of the graduation level interval to a set of input terminals of the semiconductor integrated circuit and supplying a second different input voltage corresponding to the other end of the graduation level interval to an adjacent set of input terminals of the semiconductor integrated circuit, wherein input terminals of the semiconductor integrated circuit, between said adjacent sets of input terminals and including input terminals at the closest ends of the adjacent sets, define the gradation level interval to be a test object,

said semiconductor integrated circuit outputting a plurality of gradation output voltages over said gradation level interval corresponding to said test object.

Claim **13** (new) A testing system for a display semiconductor integrated circuit outputting a plurality of gradation output voltages over a graduation level interval, comprising:

a tester power supply supplying a plurality of different input voltages to said semiconductor integrated circuit; and

a comparison judgment circuit comparing said gradation output voltages and reference voltages in order to produce a digital judgment;

said tester power supply supplying a first input voltage to at least one input terminal of the semiconductor integrated circuit and supplying a second different input voltage to another at least one input terminal in order to test gradation output voltages generated based

said tester power supply supplying a first input voltage to at least one input terminal of the semiconductor integrated circuit and supplying a second different input voltage to another at least one input terminal in order to test gradation output voltages generated based on input terminals at and between at least one less than all input terminals of the semiconductor integrated circuit.

Claim **14** (new) A testing method for semiconductor integrated circuits, said testing method performs testing of a range of gradation levels produced by the semiconductor integrated circuit by a semiconductor testing apparatus having a tester power supply and a comparison judgment circuit, comprising:

determining a gradation level interval to be the test object, from a plurality of gradation level intervals, based on the number of gradations of the semiconductor integrated circuit under test;

setting voltage values to be applied at the base power supply input terminals of said semiconductor integrated circuit based on the decided gradation level interval;

setting a judgment width according to the accuracy of the comparison judgment circuit;

designating input gradation data signals that correspond to gradation levels for the determined gradation level interval;

for each gradation level of gradation levels at and between voltages supplied to base power supply input terminals, perform digital judgment by comparison of respective gradation